EE 414 Introduction to Analog Integrated Circuits

Term Project Preliminary Design Report

**An Adjustable Voltage Regulator in 180 nm CMOS Technology**

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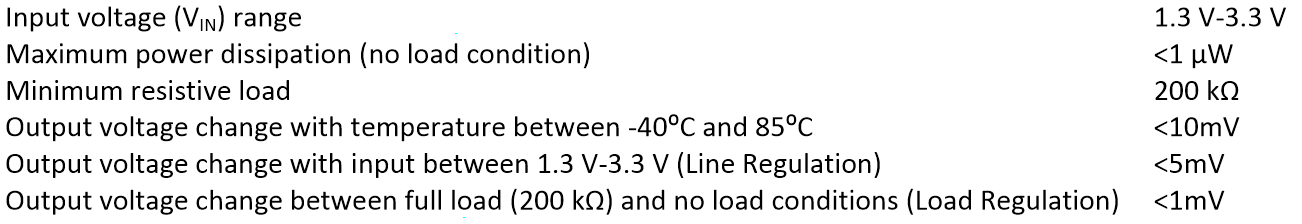
**Introduction**

In this term-project for analog IC Design course, we are required to design an adjustable voltage regulator in 180 nm CMOS technology. For this project, we are going to design a circuit which provides regulated and adjustable voltage at the output. Circuit will contain supply input, ground, adjust, and output pins. After designing the circuit we are going to implement, simulate and verify its operation. At the last step we will draw its layout in 180 nm technology. In this report, the main approach and alternative solutions to this project are proposed and explained.

**Project Description**

**GENERAL SPECIFICATIONS:**

In this term project we are required to design an adjustable voltage regulator in a 180 nm CMOS technology. We are also required to satisfy some specifications for the regulator. First of all output voltage is required to be programmed with adjust input and external resistors between 1.2 V and 0.9xVIN. Other specifications can be listed as follows:

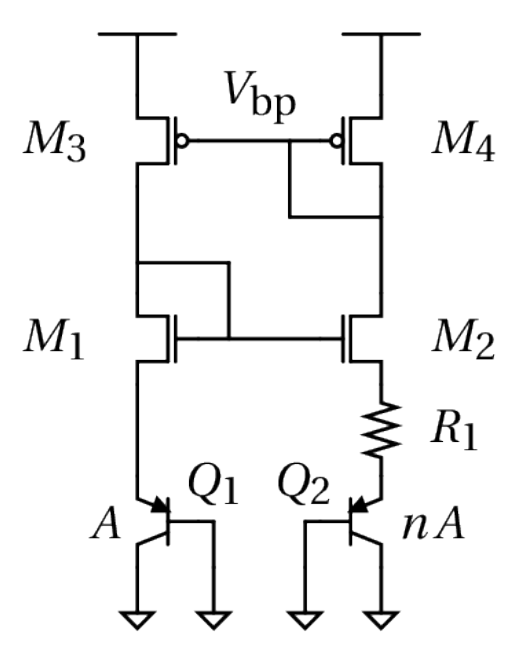
 **Figure 1 -** Specifications of the adjustable voltage regulator.

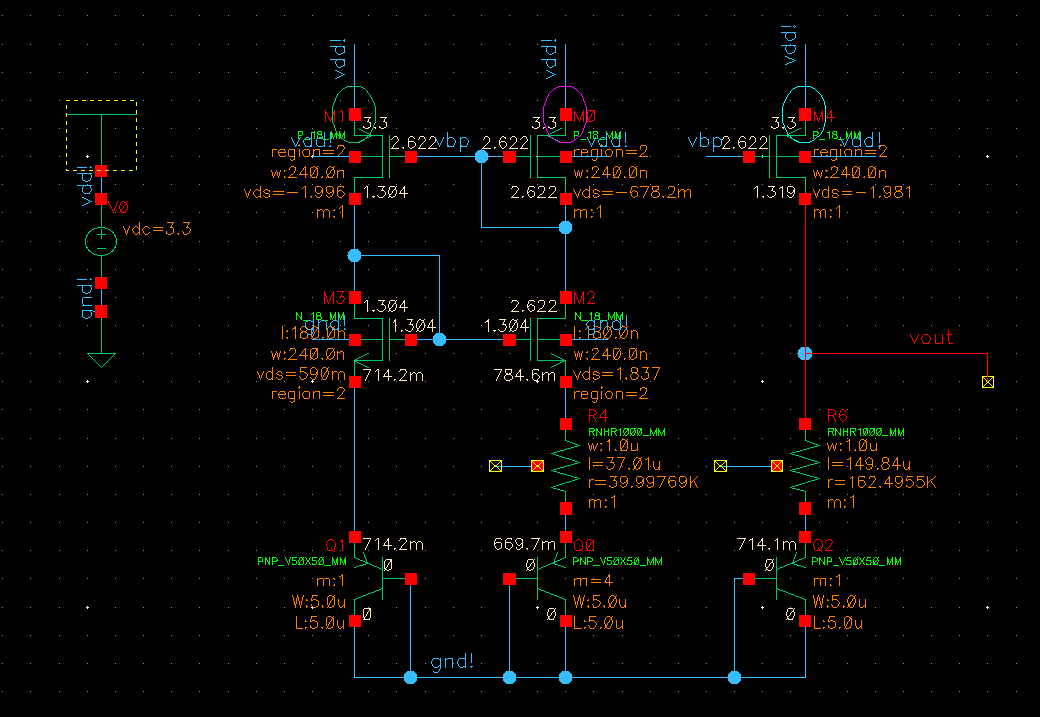
Basic principle of the operation is that, opamp works like a comparator and one of its comparison voltage is always constant, voltage reference. The other input of the opamp is also takes this value but due to feedback through the output node, this also sets the output voltage to the desired value by the help of external resistances. Here, independence of the voltage reference is very important to ensure true operation for the adjustable voltage regulator.

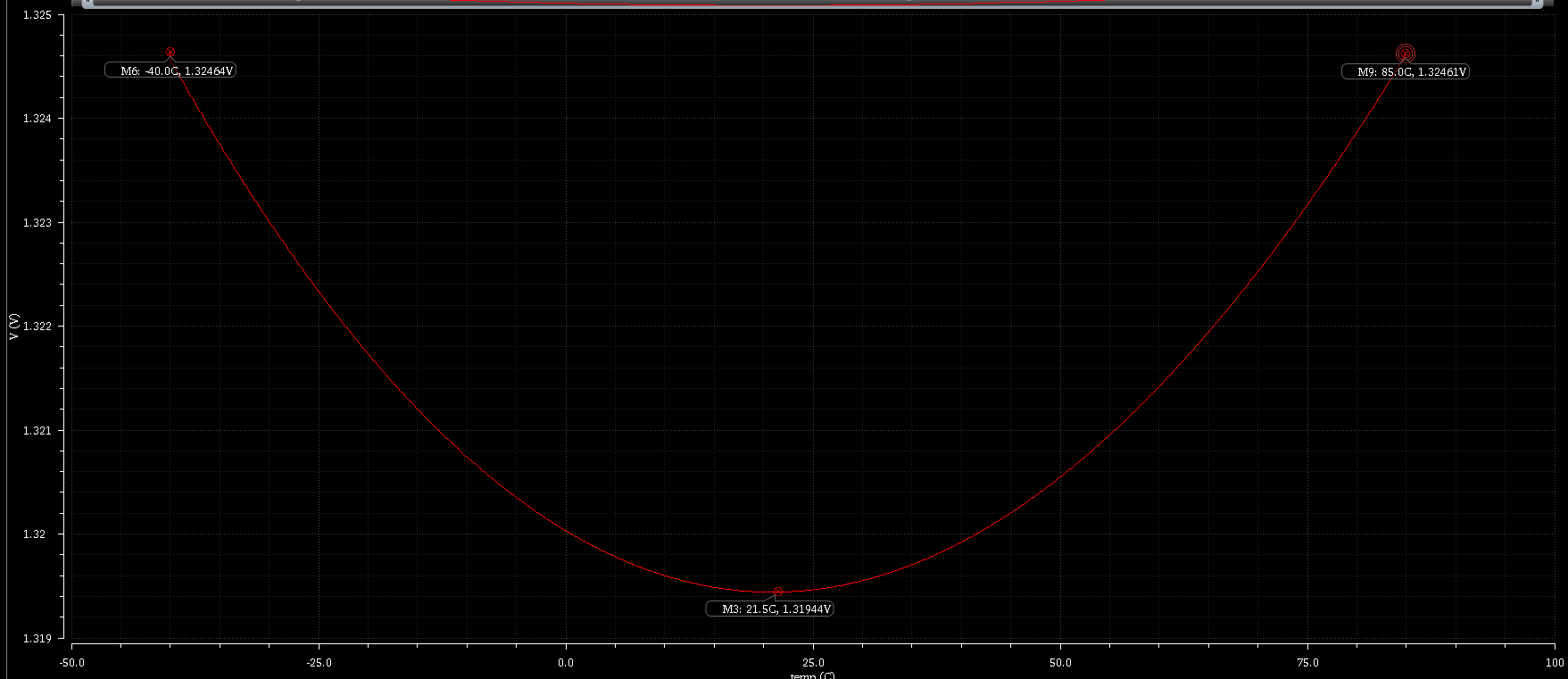
**VOLTAGE REFERENCE:**

In the first part of this project, we are going to design a voltage reference circuit to establish a reference voltage to be utilized by the op-amp in the second part. This voltage reference must be designed such that overall specifications of the project are not violated. For this purpose we need to include temperature compensation and supply independence for the given input range to our voltage reference circuit design.

Having researched over the literature, we found out that the regular voltage reference circuits are not very useful for our design specifications. First of all most of those designs include resistors and implementing resistors in CMOS process is one of the things that we should avoid, especially if the resistance values are high. Besides that issue, the basic voltage reference circuits require quite a lot power for their operation compared to our design specification of 1uW. If we use a regular band-gap voltage reference circuit such the one in **Figure 2**; both implementation of resistors and power requirements cause some trouble, even if both mathematical derivation and principles are relatively easier. In **Figure 3 & 4** implementation and simulation results for the circuit in **Figure 2** can be seen. As output voltage that circuit is quite good; however, its power consumption is above the limit and to decrease that we need to increase R1 beyond the possible dimensions for an IC design.

  
**Figure 2 –**A regular BGR circuit (Upper side: op-amp; lower side: band-gap reference)



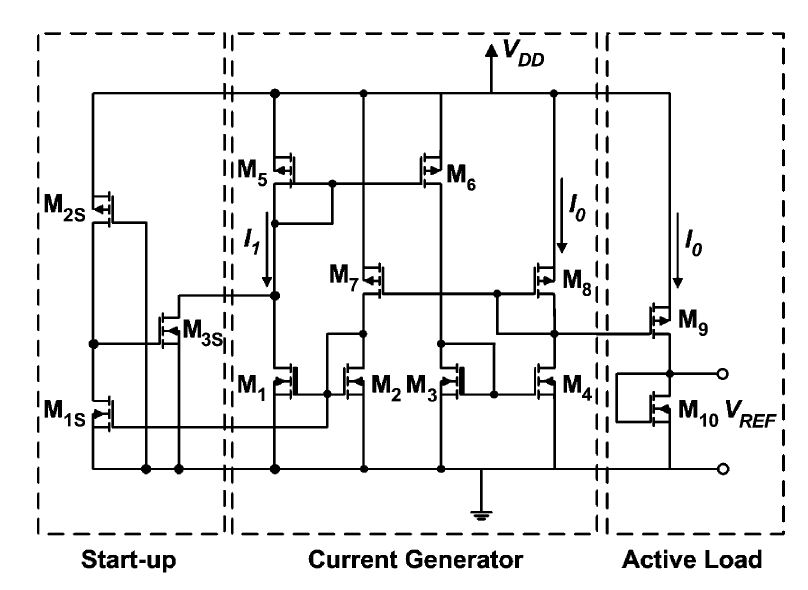


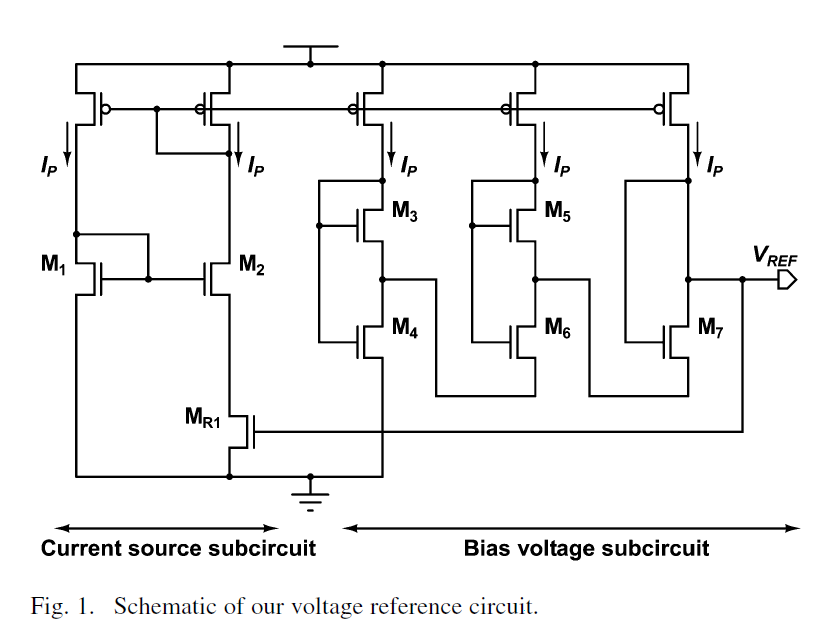
**Figure 3 –**Implementation of a regular BGR circuit

**Figure 4 –**Output voltage of the circuit in Figure 3

Therefore, we researched over the literature and decided to utilize some other architectures. Basically, our approach going to be obtaining temperature and supply independent current with a ultra-low power circuit and mirroring that current to a diode connected nMOS to obtain temperature and supply independent voltage reference.

In the **Figure 5 & 6**, examples architectures of such a circuit could be seen [1][2]. In those circuits authors utilized multistage mirrors to compensate supply and temperature variations, and obtain a well-defined voltage reference from the drain of a diode connected nMOS at the output.

  
**Figure 5 –** Voltage reference circuit proposed in [1]



**Figure 6 –** Voltage reference circuit proposed in [2]

Although the exact design parameters of circuits are not provided in [1] and [2], mathematical derivations and descriptions are explained in detail; thus, we can utilize those explanations as our initial step to design a nice reference voltage circuit.

**OPAMP:**

The second part of this project includes designing an op-amp with given specifications. Since op-amps are complicated designs and includes different stages, it is better to divide it into sub-blocks. These sub-blocks are shown as follows;

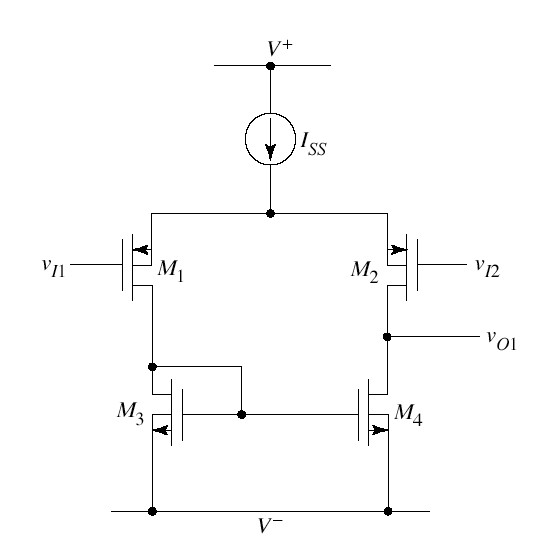
* 1st Gain Stage
* 2nd Gain Stage
* Output Stage
* Common Mode Feedback

1st and 2nd gain stages are used in order to amplify a differential signal. In these stages, number of transistors and their connection types are very important because they determine design specifications predominantly. Output stage is used as a voltage buffer and its purpose of use is to provide better load matching. Finally, common mode feedback is used in order to detect and compensate fabrication errors.

**1st Gain Stage**

In literature, one can find enormous number of different differential gain stages (1st gain stages) if he/she makes a detailed search. However, we should find and use the optimal one satisfying the design specifications of our project. The most noteworthy specification of this design is its power dissipation limit. Overall design should not dissipate more than 1 uW under no load condition. It is an absolutely small value; therefore, we should shape our design mostly on this specification.

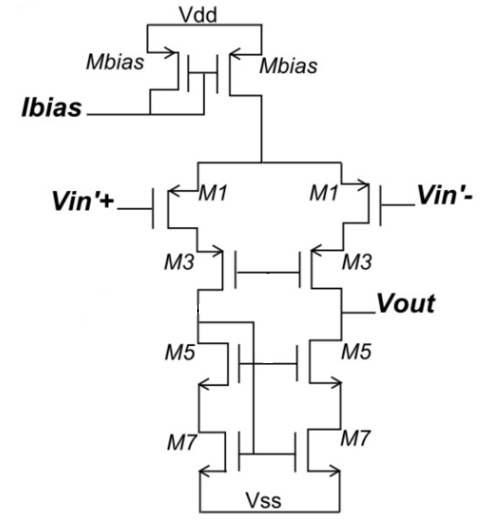
As mentioned in voltage reference part, bias voltage should be low in order to design an ultra-low power voltage reference, which means that one of the differential inputs of the op-amp should be low. Therefore, keeping the transistors in the op-amp in saturation region becomes a tough job. In order to overcome this problem, we consider to design a 1st gain stage with minimum number of transistors. Since we will not apply an AC signal to the input of the op-amp and gain specification is not very important in this project, it is not necessary to use high level gain stages. Simply, we are planning to use a 1st gain stage as shown in **Figure 7.**



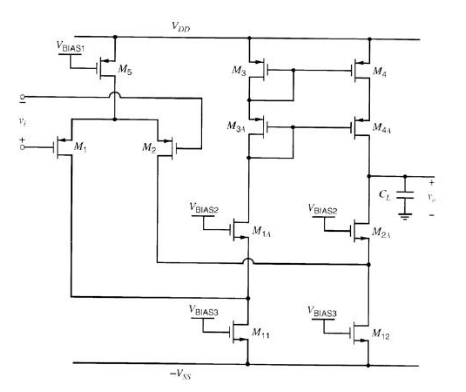
**Figure 7 –** 1st Gain Stage

In this topology, we are using only 4 MOSFETs and no resistors. Resistors cause additional power dissipation and the current produced through resistors create supply dependent output voltage, which are not desired for this project. Therefore, it is better not to use any resistors. Moreover, input voltages are given through PMOS transistors in this topology. Since the reference voltage coming from ultra-low voltage reference circuit is low, that voltage should be given to PMOS transistors instead of NMOS transistor in order to keep all the transistors in saturation region. Disadvantage of this idea might be that the current drawn from supply could be larger than the required one because VSG voltages of PMOS transistors could be large in that case. Therefore, we should adjust our reference voltage to an optimal value in order not to exceed power dissipation limit.

If this topology becomes inadequate for the 1st gain stage, we can go on to use telescopic or folded-cascode amplifier topologies. Telescopic and folded-cascode structures are shown in **Figure 8** and **Figure 9,** respectively.



**Figure 8 –** Telescopic Amplifier

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**Figure 9 –** Folded-Cascode Amplifier

These two topologies are used in order increase output resistance and gain. Since gain is not important in this project, we think that we will not need to use one of them in our design. However, if channel length modulation plays a significant role, changes the output voltage and worsens output regulation, then we may need to switch to use one of them. Since the main advantage of telescopic amplifier is gain and the main advantage of folded-cascode amplifier is voltage swing, it would be better to use folded-cascode amplifier in that case because voltage swing is more important for us.

**2nd Gain Stage**

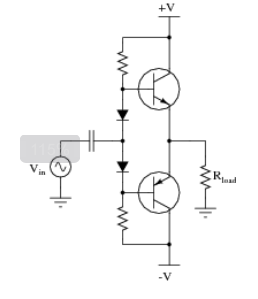
This stage is simply used for second amplification and composed of a simple common source amplifier.

**Output Stage**

This stage is one of the most critical parts of op-amp because it provides load matching. Without an output stage, output voltage of the op-amp would be significantly decreased because output resistance of gain stages is very large and load is generally much smaller than that resistance value. By voltage division, a lot of voltage would be lost without an output stage. Since the input resistance of the output stage is high whereas its output resistance is low, it creates a much smaller resistance value than load resistance when looked from load side. In this way, output voltage almost does not change with different loads.

There are different types of output stages in literature like Class-A, Class-B and Class-AB amplifiers. Class-A amplifier buffers the voltage without clamping it, but it consumes power even if there is no input to it. Therefore, the efficiency of Class-A amplifier is very low (maximum efficiency is ~%25). The efficiency of Class-B amplifier is high (maximum efficiency is ~%78.5), but it clamps the input voltage while buffering it. It is called “cross-over distortion” and a big problem especially for AC signals with low amplitude. In order to find the mid-way between Class-A and Class-B amplifiers, Class-AB amplifier were developed.

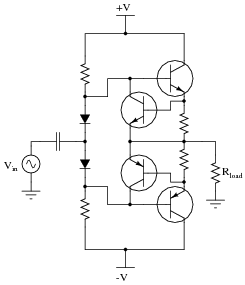
Since we will not deal with AC signals throughout this project and power dissipation is the most important specification in this project, Class-B amplifier would be a good solution for us to use it in our output stage. However, cross-over distortion might decrease our voltage swing. In order to satisfy the specifications, Class-AB might be a better solution if we will not exceed power limits. We should determine which one is better after implementing some simulations. A simple diagram of Class-AB amplifier is shown in **Figure 10.**

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**Figure 10 –** Class-AB Amplifier

In this configuration, 2 BJTs, 2 resistors and 2 diodes are used. In order to reduce power dissipation we may remove the resistors from the circuit. Diodes are used in order to reduce cross-over distortion; therefore, it is necessary to keep them in the circuit.

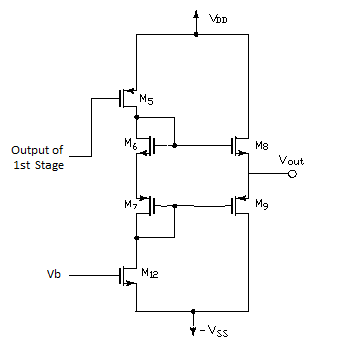
One can add an over-current protection part to the output stage of op-amp. Class-AB amplifier with over-current protection is shown in **Figure 11.**

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**Figure 11 –** Class-AB Amplifier with Over-Current Protection

2 transistors and 2 resistors are added in this topology. Therefore, we expect that the power dissipation of Class-AB amplifier will increase if we use over-current protection part. Due to the limit of power dissipation in this project, we will probably use the regular Class-AB amplifier as output stage of out op-amp.

Since npn BJT transistors cannot be implemented in a standard n-well process, we may need to use MOSFETs instead of BJTs in our design. Therefore, we should use CMOS counterpart of Class-AB amplifier if we will use standard n-well process. 2nd gain stage and CMOS counterpart of Class-AB amplifier is shown in **Figure 12.**



**Figure 12 –** CMOS Class-AB Amplifier

If power dissipation of Class-AB amplifier exceeds the limits after simulations, we may go on to use Class-B amplifier as removing the resistors and diodes in **Figure 10.**

**Common Mode Feedback**

A common mode feed-back circuit is a circuit sensing the common-mode voltage, comparing it with a proper reference, and feeding back the correcting common-mode signal (both nodes of the fully-differential circuit) with the purpose to cancel the output common-mode current component, and to fix the dc outputs to the desired level.

**Conclusion**

After simulating and verifying the operation of the layout of the proposed circuit, the project will come to an end. In this report, general solution approach is presented and investigated block by block. During this project, we are going to learn design procedures of an analog integrated circuit. Specifications are also quite tight, so that this project can be considered as cutting-edge.

**References**

[1]: De Vita, Giuseppe, and Giuseppe Iannaccone. "A sub-1-V, 10 ppm/° C, nanopower voltage reference generator." *Solid-State Circuits, IEEE Journal of* 42.7 (2007): 1536-1542.

[2]: Ueno, Ken, et al. "A 300 nW, 15 ppm/C, 20 ppm/V CMOS voltage reference circuit consisting of subthreshold MOSFETs." *Solid-State Circuits, IEEE Journal of* 44.7 (2009): 2047-2054.